SPECIFICATION

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CIRCUIT FOR PRESERVING DATA IN A FLIP-FLOP AND A METHOD OF USE RELATED APLICATION

Cross Reference to Related Applications

The present application is related to application Serial No. _____ (RPS920020084US1/2495P), filed on even date herewith, and entitled "Method and Circuit for Optimizing Power Consumption in a Flip-Flop."

Field of the Invention

[0001]   The present invention relates to logic circuits, and more particularly to a circuit for preserving state in a flip-flop during a power saving mode.

Background of the Invention

[0002]   Most VLSI designs have numerous flip-flops integrated within them. Typically, flip-flops are critical to the overall performance of this design. Conventional flip-flops are generally large, power hungry and a significant amount of time is spent optimizing their configuration. It is desirable therefore to minimize the power used by flip-flops in a circuit design. In a flip-flop design, as technologies get smaller, it is harder to control the amount of leakage current provided thereby. Therefore, it is desirable to make device sizes smaller within the flip-flop at the same time being able to preserve the state of whatever contents are within the flip-flop. It is known that one way to save power is to shut off sections of the design. For example, one way to save power is to utilize clock gating to disable the clock when it is not used. Also, in an effort to save or minimize standby power, some designs have resorted to disabling non-used sections of the design from the power supply. However, disabling the power supply generally results in a loss of stored data in the volatile memory elements.

[0003]   One solution for this problem is to transfer the data or state of the latch to an on-chip memory before the latch is disconnected from the power supply. Examples of chip memory include SRAM, DRAM or flash memory. This technique, however, requires an auxiliary device to preserve the state, which adds cost and adds to the overall size of the design of the device.

[0004]   Accordingly, what is needed is a method and circuit for preserving data in a flip-flop while also conserving power. The method and circuit should also be cost effective, save space, and easily implemented in existing circuit designs. The present invention addresses such needs.

Summary of Invention

[0005]   A flip-flop is disclosed in which power consumption is reduced in a standby mode. In a first aspect, the flip-flop comprises a first latch adapted to be coupled to a first power supply and a second latch coupled to the first latch and adapted to be coupled to a second power supply. The first and second power supplies are independently controllable to minimize power consumption in a standby mode.

[0006]   In a second aspect, a flip-flop comprises a first latch adapted to be coupled to a first power supply. The first latch receives at least one bit. The flip-flop includes a second latch coupled to the first latch and adapted to be coupled to a second power supply. The second latch stores the at least one bit from the first latch. The size of the second latch is minimized to reduce power consumption. The flip-flop also includes a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a clock to the multiplexor is active and for outputting the at least one bit from the second latch when the clock is inactive. The first and second power supplies are independently controllable.

[0007]
           In a third aspect, a method for minimizing the power consumption of a flip-flop is also disclosed. The flip-flop includes a first latch and a second latch coupled thereto. The method comprises providing a first independently controllable power supply coupled to the master latch; and providing a second independently controllable power supply coupled to the slave latch. The method further includes reducing the voltage of at least one of the first and second power supplies responsive to the detection of a
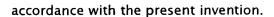
power saving mode.

[0008]   An additional feature of the present invention is a restore mechanism which multiplexes the data and an output of a slave latch of a master/slave FF to enable recovery of the state of the contents of the master latch.

[0009]   Finally, another feature of the present invention is a state latch which is coupled to the second power supply and is only activated upon detection of standby power saving mode to retain the contents of the master latch.

[0010]   Hence, a simple means to optimize power consumption in random logic latch configurations with or without clock gating has been disclosed. According to the method and circuit disclosed herein, the present invention provides numerous benefits. For example, it preserves the data in a FF during a power savings mode.

Brief Description of Drawings

[0011]   FIG. 1 illustrates a conventional logical configuration employing a pair of L1/L2 master/slave latches coupled to logic.

[0012]   FIG. 2 illustrates a conventional logical configuration with voltage supplies, V1 and V2, connected to the master latch and the slave latch respectively

[0013]   FIG. 3 is a flow chart showing a method for conserving standby power in a logical configuration of FIG. 2.

[0014]   FIG. 4 is a block diagram of a conventional master-slave flip-flop (FF).

[0015]   FIG. 5A is a high-level block diagram of the FF in accordance with that application.

[0016]   FIG. 5B is a timing diagram showing the various signals of FF of FIG. 4A

[0017]   FIG. 6 is a schematic diagram of a master-slave FF, in accordance with the present invention.

[0018]   FIG. 7 is a schematic diagram of a master-slave FF which includes an additional multiplexor.

[0019]
    FIG. 8 is a schematic diagram of a master-slave FF' which includes a state latch in

accordance with the present invention.

[0020]   FIG. 9 is a flowchart which illustrates a method enabling power saving mode utilizing FF.

[0021]   FIG. 10 is a flowchart which illustrates a method for returning to normal mode from power saving mode utilizing FF.

Detailed Description

[0022]   The present invention relates to logic circuits, and more particularly to a method and circuit for preserving data in a flip-flop during a power saving mode. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

[0023]   FIG. 1 illustrates a conventional logical configuration 10 employing a pair of L1/L2 master/slave FFs 12 and 14 coupled to logic 16. In this embodiment, the content of the second L1 18 will be consistent with logic 16 and the content of the first L2 17 upon reactivation of the clock C2 in an un-gated clocking methodology. The logic is designed between the L2 stage of one FF12 and the L1 stage of the other of master FF14. The Shift Register chain is formed by connecting the L2 output of one SRL to the Scan In of another. The Cycle Time is designed from the launch of clock C2 to fall of clock C1.

[0024]   In the conventional logical configuration, each of the slave-master FF 12 and 14 typically has one power supply connected thereto that controls the overall voltage. In a first aspect of the present invention, each of the flip-flop pairs would have an independent voltage supply coupled thereto. FIG. 2 illustrates a conventional logical configuration 100 with voltage supplies, V1 and V2, connected to the master latch and the slave latch respectively. Each of the voltage supplies is independently controllable. They could, in fact, be of the same voltage level therefore. When a power-saving

is encountered and the clocks are disabled, at least one of the voltage supplies can be reduced from its full value to a minimum value, and the latch then is retaining the state of the contents could be kept at a value to sustain the state. In so doing, the overall power consumption of the logical configuration will be significantly reduced.

[0025]   FIG. 3 is a flow chart showing a method for conserving standby power in a logical configuration of Fig. 2. First, a power saving mode is detected via step 352. Next, all clocks related to the flip-flop are disabled via step 354. Next, the voltage supply related to one of the flip-flops is reduced to zero, via step 356. Finally, the other of the two voltage supplies is reduced to a voltage which will preserve the state of contents of the other of the flip-flops, via step 358.

[0026]   By way of providing independently controllable voltage supplies on each of the master latch and slave latch of the FF, the standby power and therefore leakage current of a conventional master/slave flip-flop arrangement is significantly reduced. However, it is desirable to be able to further reduce the standby power while also preserving the state of the contents of the device. For a further description of the problem with conventional flip-flops in conserving power refer now to the following discussion in conjunction with FIG. 4.

[0027]   Fig. 4 is a block diagram of a conventional master-slave flip-flop (FF) 408. The FF 408 includes a master latch 410 and a slave latch 412. In operation, the master latch 410 receives data (labeled "data"), a clock pulse C1, and a clock set pulse C1B. The slave latch 412 receives a clock pulse C2 and a clock set pulse C2B. The slave latch 412 outputs the data (labeled "L2out"). The clock pulse C1 is driven by a clock C1. Similarly, the clock pulse C2 is driven by a clock C2.

[0028]   With regard to performance, there are set-up criteria for the master latch and launch criteria for the slave latch. The sum of the set up criteria and the launch criteria provide the most performance critical information. The objective is to minimize the time needed to transfer data from the master latch 410 to the slave latch 412. Various latching configurations can be employed, but all generally use a write-thru-read approach. That is, the architecture of the slave latch 412 is such that it stores the incoming data while it is outputting the data. For more performance, the device sizes of the slave latch 412 are generally large enough to support high-speed data transfer.

As such, the large device sizes result in increased capacitance and larger area, hence they consume more power.

[0029] Co-pending U.S. patent application serial number _____ [RPS920020084US1/2495P]," filed on even date herewith, and entitled "Method and Circuit for Optimizing Power Consumption in a Flip-Flop," which is incorporated in its entirety herein, discloses a flip-flop in which power consumption is substantially minimized. The features of the flip-flop are described below in conjunction with the accompanying figures.

[0030] Fig. 5A is a high-level block diagram of the FF 500 in accordance with that application. The FF 500 includes a master latch 510, a slave latch 512, and a multiplexor 514. As is seen, X, Y and Z nodes are identified. The actual configuration of the master latch 510 and the slave latch 512 can vary and will depend on the specific embodiment. In this embodiment, the multiplexor 514 is a shunt multiplexor.

[0031] Because the slave latch 512 does not serve a performance-critical function, it can be implemented utilizing minimum sized devices. By minimizing the size of the devices within the slave latch, the leakage current and the operating current is significantly reduced as compared to the larger conventional slave latch. As a result, the overall power consumption of the FF 500 is optimized.

[0032] Fig. 5B is a timing diagram showing the various signals of FF 500 of Fig. 5A. As is seen, clock C1 is shown as a first waveform, clock C2 is shown as a second waveform, and data is shown as a third waveform. As is also seen, the waveforms of the X, Y and Z nodes are shown. Referring now to both Figs. 5A and 5B together, when the data is received by the master latch 510, it is passed to node X when the clock C1 goes high. The data is received by both the slave latch 512 and the multiplexor 514. Assuming the previous states of nodes Y and Z were a logical low, the state at both nodes Y and Z go high (shown in FIG. 5B at 552 and 554, respectively) when the clock C2 goes high. As shown in the timing diagram, node Z changes at a significantly faster rate than does node Y. The signal at node Y changes at a slower rate than the signal at node Z because the slave latch 512 includes gates therewithin that consume less power since the slave latch 512 uses all minimum devices. The slave latch can be designed in this manner because it is not in the performance critical path.

[0033]   Utilizing the flip-flop 500, the slave latch 512 is not involved in the critical

performance, and the device sizes there within can be a minimum size. In addition,

the slave latch 512 can now be coupled to an auxiliary power supply rather than a

main power supply. Therefore, a system and method in accordance with the present

invention utilizes a power-consumption optimized flip-flop in conjunction with a

dual-voltage system in which the state of the contents can be preserved while a power

supply is disabled. In so doing, standby power can be substantially reduced while

preserving the state of the contents. For a more detailed description of the features of

this portion of the present invention, refer now to the following discussion in

conjunction with the accompanying figures.

[0034]   Fig. 6 is a schematic diagram of a master-slave FF 600, in accordance with the

present invention. The FF 600 includes a master latch 602 that is coupled to a slave

latch 604. The master latch 602 is coupled to a first voltage supply 607 and the slave

latch 604 is coupled to a second voltage supply 609.

[0035]   In the master latch 602, the parallel connected pair of transmission devices 603

forms a first multiplexor there within. Depending upon the state of the SE signal,

either the D (data) input or the I (scan) input will be presented to the master latch 602

for loading when the clock C1 is activated. The clusters of transistors comprising the

master latch 602 are as follows: two sets of four device series configuration of two

series pfets and two series nfets whose respective outputs are at the pfet-nfet

junction shown at 610 and 612, respectively, and an inverter 615. These two sets 610

and 612 of four devices have their outputs commoned and have their respective

controls swapped and thus act as a multiplexor. The first series set 610 passes the

inverse of the value presented from the transmission gate pair 603 (D or I mux) when

the clock C1 is active. The second set 612 is inactive when the first set 610 is active

and vice-versa to provide the appropriate contents to the output. When the clock C1 is

inactive, the first set 610 is essentially tri-stated and blocks the input choice from

changing the content of the latch. The second set 612 activates and provides the

necessary feedback to form the latch. The slave latch 604 comprises the two

transistor pair 650 which is coupled to a set of four transistors 652.

[0036]
          The transmission device 608 between the master and slave latches 602 and 604,

respectively, which has its nfet and pfet gate nodes connected to clock C2 and clock C2B, respectively, transfers the content held in the master latch 602 to the slave latch 604 when the clock C2 and clock C2B are active; otherwise, the two latches are isolated from one another.

[0037]   The basic premise is that the voltage supply 607 can be reduced to 0-volts when a static power saving mode is to be entered, while voltage supply 609 will be kept at a sufficient bias to maintain the state of the latch. Since the master latch is comprised larger performance devices, shutting off the voltage supply 607 will result in significant standby/leaking current reduction. The slave latch 604 is comprised of all minimum devices and as such results in far less leakage relative to the master latch 602. If additional leakage reduction is desired, the voltage supply 609 can be reduced to a level that allows the slave latch 604 to retain value at less leakage. Note also that the clock C2 inverter is also connected to the voltage supply 609, whereas the clock C1 circuitry and the clock C1 generation circuitry are coupled to the supply at voltage supply 607.

[0038]   The FF 600 can be utilized to advantage when different clock gating configurations are used. The use of FF 600 in each of these configurations will be described in detail herein below.

[0039]   The specific clock-gating configuration will vary and will depend on the specific application. For example, there can be four different clock-gating embodiments as follows:

[0040]   Case A: the clock C2 and the clock C1 are free running;

[0041]   Case B: the clock C2 is gated and the clock C1 is free running;

[0042]   Case C: the clock C2 is free running and the clock C1 is gated; and

[0043]   Case D: the clock C1 and the clock C2 are gated.

[0044]   The present invention readily applies to the embodiments of Cases A, B, C, and D.

[0045]   CASE A: THE CLOCK C2 AND THE CLOCK C1 ARE FREE RUNNING :

[0046]   Referring back to FIG. 6, for example, in Case A, both the clock C1 and the clock

C2 are free running, and as such, the content of the master latch 602 and the slave latch 604 are the same at the conclusion of the cycle. Hence, if the cycle is initiated by the arrival of a launch or the clock C2 pulse, and if the cycle is terminated by a capture or the clock C1 pulse, the content of both the master latch 602 and the slave latch 604 will be the same on the arrival of the next clock C2 pulse.

[0047]   After the arrival of the next clock C2 pulse, the steps for power saving described above can be applied. The master latch 602 will lose its content. The slave latch 604, however, will retain its content.

[0048]   Upon awakening from the power saving mode, power is restored to voltage supply 607. Also, the voltage supply 609 is restored to its full value, if its voltage had been decreased to reduce leakage. Upon satisfactory restoration of the power supplies, the clock C1 is activated, thereby restoring the prior state in the master latch 602 from the slave latch 604.

[0049]   CASE B: THE CLOCK C2 IS GATED AND THE CLOCK C1 IS FREE RUNNING.

[0050]   The embodiments of Case B operate similarly to those embodiments of Case A. Referring still to FIG. 6, because the clock C2 is gated, the master latch 602 contains valid data from a prior cycle. Upon awakening from a standby power saving mode, i.e., returning to a normal mode, the master latch 602 is reloaded with its prior content from the logic being fed by another slave latch (not illustrated), which is located logically upstream from the master latch 602.

[0051]   CASE C: THE CLOCK C2 IS FREE RUNNING AND TEH CLOCK C1 IS GATED.

[0052]   FIG. 7 is a schematic diagram of a master-slave FF 600' which includes an additional multiplexor 702. The slave latch 604' is refreshed by the master latch 602' on each cycle, regardless of whether the content of the master latch 602' has changed. To enable recovery of the state of the master latch 602' after a power down cycle of the voltage supply 607', the logic configuration includes a restore feature. This restore feature employs the multiplexor 702, which multiplexes the normal data and the output of the slave latch 604'. The multiplexor 702 can multiplex a LSSD scan input and the output of the slave latch 604' to provide higher performance. The size of all these devices can be minimized because they do not impact performance.

[0053]   The slave latch 604' retains its state in standby mode. Upon awakening from the standby power saving mode, before the clocks can be reactivated, a restore signal goes active to steer the content of the slave latch 604' into the multiplexor 702. The multiplexor 702 can be configured to steer either a scan input or the slave latch 604' output to the scan input of the master latch 602' as is illustrated in Figure 7. An alternative approach could use multiplexor 702 to steer either primary data or the slave latch 604' output to the data input (D) of the master latch 602'. This choice will depend upon the specific application. In the example cited and illustrated in Figure 7, the restore signal is activated along with the scan enable (SE) before the C1 clock is activated. Upon successful restoration of the slave latch 604', the restore signal and SE can be disabled.

[0054]   CASE D: THE CLOCK C1 AND THE CLOCK C2 ARE GATED.

[0055]   FIG. 8 is a schematic diagram of a master-slave FF 600" which includes a state latch 816 in accordance with the present invention. In case D, the local content of the master latch 602" can be different from the content of the slave latch 604". Accordingly, Case D is more complex than Cases A-C. The state latch 816 is coupled to the V2 supply and is only activated upon detection of standby power saving mode. In fact, state latch 816 can be coupled to the voltage supply 609" through a header switch to eliminate active power in normal, functional mode. Also, the state latch 816 has minimum-sized device geometries.

[0056]   The master-slave FF 600" operates in a functional mode no differently than without the state saving condition. The feedback components include the multiplexor 702' and the state latch 816. In one embodiment, the multiplexor 702' and the state latch 816 can be integrated to save space. They can also share resources. Also, the content of the master latch 602" can be different from the content of the slave latch 604". Also, the contents of both the master latch 602" and the slave latch 604" are preserved. The state latch 816 is activated by a state saving clock signal upon detection of entry into a power saving mode.

[0057]   Figure 9 is a flowchart which illustrates a method enabling power saving mode utilizing FF 600". A power saving mode is detected, via step 902. Next, all clocks are stopped, via step 904. Then, a state saving clock is enabled to load the master latch

contents into the state latch 816, via step 906. Next, the supply voltage 607" is reduced from its full value V1max to 0V, via step 908. Finally, the supply voltage 609" is reduced from its full value V2max to a minimum voltage V1min to sustain the state, via step 910. (Note that the specific value of Vmin will vary and will depend on the specific application.

[0058]   Figure 10 is a flowchart which illustrates a method for returning to normal mode from power saving mode utilizing FF 600". First, a return from the standby power saving mode is detected, via step 1002. Next, the supply voltage 609" is restored V2min to its full value V2max, via step 1004. Then, the supply voltage 607" is restored from 0V to its full value V1max, via step 1006. Next, a restore signal is activated, via step 1008. Then, an SE signal is activated if the restore signal is coupled to the I-port of the master latch, via step 1010. The state saving clock signal is deactivated, via step 1012. The clock C2 is restored, via step 1014. The SE signal (which may be different depending on implementation) is deactivated, via step 1016. Finally, normal clock sequence is resumed, via step 1018.

[0059]   Hence, a simple means to optimize power consumption in random logic latch configurations with or without clock gating has been disclosed. According to the method and circuit disclosed herein, the present invention provides numerous benefits. For example, it preserves the data in a FF during a power savings mode.

[0060]   Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.